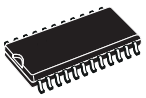
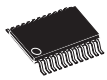
74LVX4245

OCTAL DUAL SUPPLY BUS TRANSCEIVER

- HIGH SPEED:
  t_{PD} = 8.5 ns (MAX.) at
  V_{CCA}=5.0V V_{CCB} = 3.3V
- LOW POWER DISSIPATION:
  I_{CCA} = I_{CCB} =5µA(MAX.) at T_A=25°C
- LOW NOISE: V_{OLP} =0.3V (TYP.) at
  V_{CCA}=5.5V V_{CCB}=3.3V
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}|$ = I_{OL} = 24mA (MIN)
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
  V_{CCA}(OPR) = 4.5V to 5.5V (1.2V Data Retention)
  V_{CCB}(OPR) = 2.7V to 3.6V (1.2V Data Retention)
  PIN AND FUNCTION COMPATIBLE WITH
  74 SERIES 4245
- IMPROVED LATCH-UP IMMUNITY



SOP



TSSOP

ORDER CODES

PACKAGE	TUBE	T & R
SOP	74LVX4245M	74LVX4245MTR
TSSOP		74LVX4245TTR

DESCRIPTION

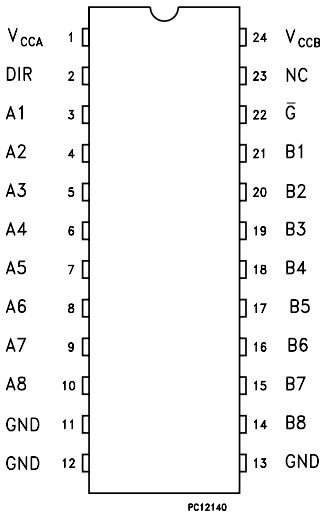
The 74LVX4245 is a dual supply low voltage CMOS OCTAL BUS TRANSCEIVER fabricated with sub-micron silicon gate and double-layer metal wiring C^2MOS technology. Designed for use as an interface between a 5V bus and a 3.3V bus in a mixed 5V/3.3V supply systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

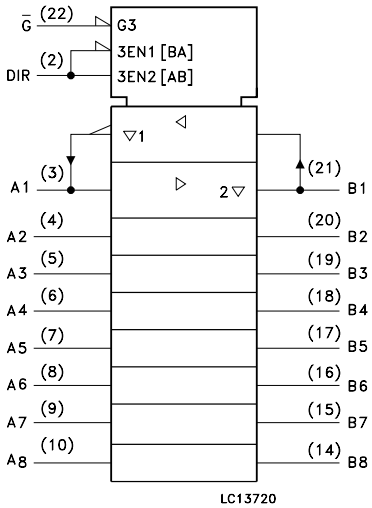
This IC is intended for two-way asynchronous communication between data buses and the direction of data transmission is determined by DIR input. The enable input $\overline{G}$ can be used to disable the device so that the buses are effectively isolated.

The A-port interfaces with the 5V bus, the B-port with the 3.3V bus.

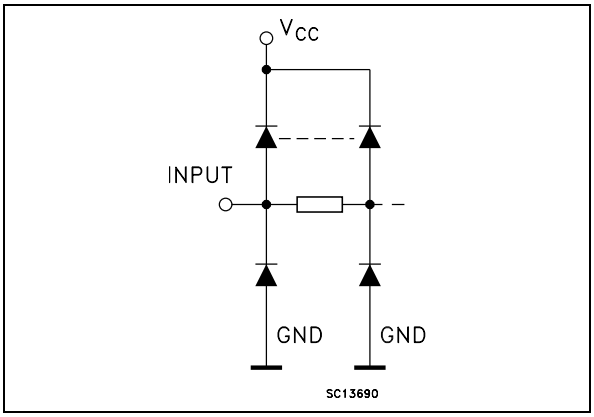
All inputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS





INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME QND FUNCTION
2	DIR	Directional Control
3, 4, 5, 6, 7, 8, 9, 10	A1 to A8	Data Inputs/Outputs
21, 20, 19, 18, 17, 16, 15, 14	B1 to B8	Data Inputs/Outputs
22	$\overline{G}$	Output Enable Input
11, 12, 13	GND	Ground (0V)
23	NC	Not Connected
1	V_{CCA}	Positive Supply Voltage
24	V_{CCB}	Positive Supply Voltage

TRUTH TABLE

INPUTS		FUNCTION		OUTPUT
$\overline{G}$	DIR	A BUS	B BUS	
L	L	OUTPUT	INPUT	A = B
L	H	INPUT	OUTPUT	B = A
H	X	Z	Z	Z

X : Don't Care
Z : High Impedance

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CCA}	Supply Voltage	-0.5 to +7.0	V
V_{CCB}	Supply Voltage	-0.5 to +7.0	V
V_I	DC Input Voltage	-0.5 to V_{CCA} + 0.5	V
$V_{I/OA}$	DC I/O Voltage	-0.5 to V_{CCA} + 0.5	V
$V_{I/OB}$	DC I/O Voltage	-0.5 to V_{CCB} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 50	mA
I_{OA}	DC Output Current	± 50	mA
I_{OB}	DC Output Current	± 50	mA
I_{CCA}	DC V_{CC} or Ground Current	± 200	mA
I_{CCB}	DC V_{CC} or Ground Current	± 100	mA
P_d	Power Dissipation	180	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CCA}	Supply Voltage (note 1)	4.5 to 5.5	V
V_{CCB}	Supply Voltage (note 1)	2.7 to 3.6	V
V_I	Input Voltage	0 to V_{CCA}	V
$V_{I/OA}$	I/O Voltage	0 to V_{CCA}	V
$V_{I/OB}$	I/O Voltage	0 to V_{CCB}	V
T_{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time (note 2)	0 to 10	ns/V

1) V_{IN} from 30% to 70% of V_{CC}
2) V_{CCA} = 4.5 to 5.5V; V_{CCB} = 2.7 to 3.6V;

DC SPECIFICATIONS FOR V_{CCA}

Symbol	Parameter	Test Condition			Value							Unit
		V_{CCA} (V)	V_{CCB} (V)		T_A = 25 °C			-40 to 85 °C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IHA}	High Level Input Voltage	4.5	3.3		2.0			2.0		2.0		V
		5.5	3.3		2.0			2.0		2.0		
V_{ILA}	Low Level Input Voltage	4.5	3.3				0.8		0.8		0.8	V
		5.5	3.3				0.8		0.8		0.8	
V_{OHA}	High Level Output Voltage	4.5	3.0	I_O=-100 µA	4.4	4.5		4.4		4.4		V
		4.5	3.0	I_O=-24 mA	3.86			3.76		3.76		
V_{OLA}	Low Level Output Voltage	4.5	3.0	I_O=100 µA		0	0.1		0.1		0.1	V
		4.5	3.0	I_O=24 mA			0.36		0.44		0.44	
I_{IA}	Input Leakage Current	5.5	3.6	V_I = V_{CC} or GND			± 0.1		± 1		± 1	µA
I_{OZA}	High Impedance Output Leakage Current	5.5	3.6	V_{IA} = V_{IHA} or V_{ILA} V_{IB} = V_{IHB} or V_{ILB} $V_{I/OA}$ = V_{CCA} or GND			± 0.5		± 5		± 5	µA
I_{CCtA}	Quiescent Supply Current	5.5	3.6	V_{IA} = V_{CCA} or GND V_{IB} = V_{CCB} or GND			5		50		50	µA
ΔI_{CCtA}	Maximum Quiescent Supply Current / Input (An, DIR, $\overline{G}$)	5.5	3.6	V_{IA} = V_{CCA} - 2.1V V_{IB} = V_{CCB} or GND			1.35		1.5		1.5	mA

DC SPECIFICATIONS FOR V_{CCB}

Symbol	Parameter	Test Condition			Value							Unit
		V_{CCA} (V)	V_{CCB} (V)		T_A = 25 °C			-40 to 85 °C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IHB}	High Level Input Voltage	5.0	3.6		2.0			2.0		2.0		V
		5.0	2.7		2.0			2.0		2.0		
V_{ILB}	Low Level Input Voltage	5.0	3.6				0.8		0.8		0.8	V
		5.0	2.7				0.8		0.8		0.8	
V_{OHB}	High Level Output Voltage	4.5	3.0	I_O=-100 µA	2.9	3.0		2.9		2.9		V
		4.5	3.0	I_O=-12 mA	2.48			2.4		2.4		
		4.5	2.7	I_O=-8 mA	2.26			2.2		2.2		
V_{OLB}	Low Level Output Voltage	4.5	3.0	I_O=100 µA		0.0	0.1		0.1		0.1	V
		4.5	3.0	I_O=12 mA			0.31		0.40		0.40	
		4.5	2.7	I_O=8 mA			0.31		0.40		0.40	
I_{IB}	Input Leakage Current	5.5	3.6	$V_I = V_{CCA}$ or GND			± 0.1		± 1		± 1	µA
I_{OZB}	High Impedance Output Leakage Current	5.5	3.6	$V_{IA} = V_{IHA}$ or V_{ILA} $V_{I/Ob} = V_{CCb}$ or GND			± 0.5		± 5		± 5	µA
I_{CCtB}	Quiescent Supply Current	5.5	3.6	$V_{IA} = V_{CCA}$ or GND $V_{IB} = V_{CCB}$ or GND			5		50		5	µA
ΔI_{CCtB}	Maximum Quiescent Supply Current / Input	5.5	3.6	$V_{IA} = V_{CCA}$ or GND $V_{IB} = V_{CCB}$ - 0.6V			0.35		0.5		0.35	mA

DINAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition			Value							Unit
		V_{CCA} (V)	V_{CCB} (V)		T_A = 25 °C			-40 to 85 °C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{OLPA}	Dynamic Low Level Quiet Output (note 1, 2)	5.0	3.3			1.0	1.5					V
		5.0	3.3		-1.2	-0.6						
V_{OLPB}	Dynamic Low Level Quiet Output (note 1, 2)	5.0	3.3			0.8	1.2					V
		5.0	3.3		-0.8	-0.5						
V_{IHDA}	Dynamic High Voltage Input (note 1, 3)	5.0	3.3				2					V
V_{ILDA}	Dynamic Low Voltage Input (note 1, 3)	5.0	3.3		0.8							V
V_{IHDB}	Dynamic High Voltage Input (note 1, 3)	5.0	3.3				2					V
V_{ILDB}	Dynamic Low Voltage Input (note 1, 3)	5.0	3.3		0.8							V

1) Worst case package
2) Max number of output defined as (n). Data inputs are driven 0V to 3.3V, (n-1) outputs switching and one output at GND
3) Max number of data inputs (n) switching. (n-1) switching 0V to 3.3V. Inputs under test switching: 3V to threshold (V_{ILD}). 0V to threshold (V_{IHD}) f = 1MHz

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 3ns)

Symbol	Parameter	Test Condition		Value (3)							Unit
		V_{CCB} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay Time (An to Bn)	2.7					1.0	10.0	1.0	11.0	ns
		3.0(*)		1.0	5.1	8.5	1.0	9.0	1.0	10.0	
t_{PHL}	Propagation Delay Time (An to Bn)	2.7					1.0	10.0	1.0	11.0	
		3.0(*)		1.0	5.3	8.5	1.0	9.0	1.0	10.0	
t_{PZL}	Output Enable Time ($\overline{G}$ to Bn)	2.7					1.0	11.5	1.0	12.5	ns
		3.0(*)		1.0	6.5	10.0	1.0	10.5	1.0	11.5	
t_{PZH}	Output Enable Time ($\overline{G}$ to Bn)	2.7					1.0	11.5	1.0	11.5	
		3.0(*)		1.0	6.7	10.0	1.0	10.5	1.0	11.5	
t_{PLZ}	Output Disable Time ($\overline{G}$ to Bn)	2.7					1.0	10.0	1.0	11.0	ns
		3.0(*)		1.0	6.0	9.5	1.0	10.0	1.0	11.0	
t_{PHZ}	Output Disable Time ($\overline{G}$ to Bn)	2.7					1.0	7.5	1.0	8.5	
		3.0(*)		1.0	3.3	6.5	1.0	7.0	1.0	8.0	
t_{PLH}	Propagation Delay Time (Bn to An)	2.7					1.0	10.0	1.0	11.0	ns
		3.0(*)		1.0	5.4	8.5	1.0	9.0	1.0	10.0	
t_{PHL}	Propagation Delay Time (Bn to An)	2.7					1.0	10.0	1.0	11.0	
		3.0(*)		1.0	5.5	8.5	1.0	9.0	1.0	10.0	
t_{PZL}	Output Enable Time ($\overline{G}$ to An)	2.7					1.0	10.0	1.0	11.0	ns
		3.0(*)		1.0	5.2	9.0	1.0	9.5	1.0	10.5	
t_{PZH}	Output Enable Time ($\overline{G}$ to An)	2.7					1.0	10.0	1.0	11.0	
		3.0(*)		1.0	5.8	9.0	1.0	9.5	1.0	10.5	
t_{PLZ}	Output Disable Time ($\overline{G}$ to An)	2.7					1.0	7.5	1.0	8.5	ns
		3.0(*)		1.0	3.9	7.0	1.0	7.5	1.0	8.5	
t_{PHZ}	Output Disable Time ($\overline{G}$ to An)	2.7					1.0	7.5	1.0	8.5	
		3.0(*)		1.0	2.9	6.5	1.0	7.0	1.0	8.0	
t_{OSLH} t_{OSHL}	Output To Output Skew Time (note1, 2)	2.7			0.5	1.0		1.5		1.5	ns
		3.3(**)			0.5	1.0		1.5		1.5	

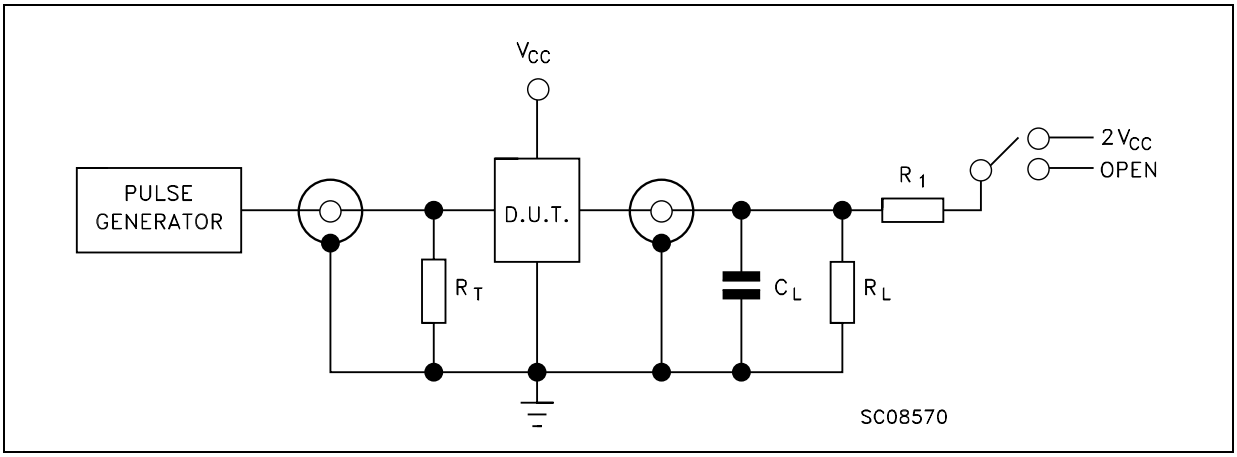
1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ($t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$
2) Parameter guaranteed by design
3) Typical values at V_{CCA} = 5.0V, V_{CCB} = 3.3V
(*) Voltage range is 3.0V ± 0.3V

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition			Value							Unit
		V_{CCA} (V)	V_{CCB} (V)		T_A = 25 °C			-40 to 85 °C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C_{INA}	Input Capacitance	open	open			4.5	10		10		10	V
$C_{I/O}$	Input/Output Capacitance	3.3	5.0			10						V
C_{PD}	Dynamic Low Level Quiet Output (note 1) A to B	3.3	5.0			55						V
C_{PD}	Dynamic Low Level Quiet Output (note 1) B to A	3.3	5.0			40						V

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8$ (per circuit)

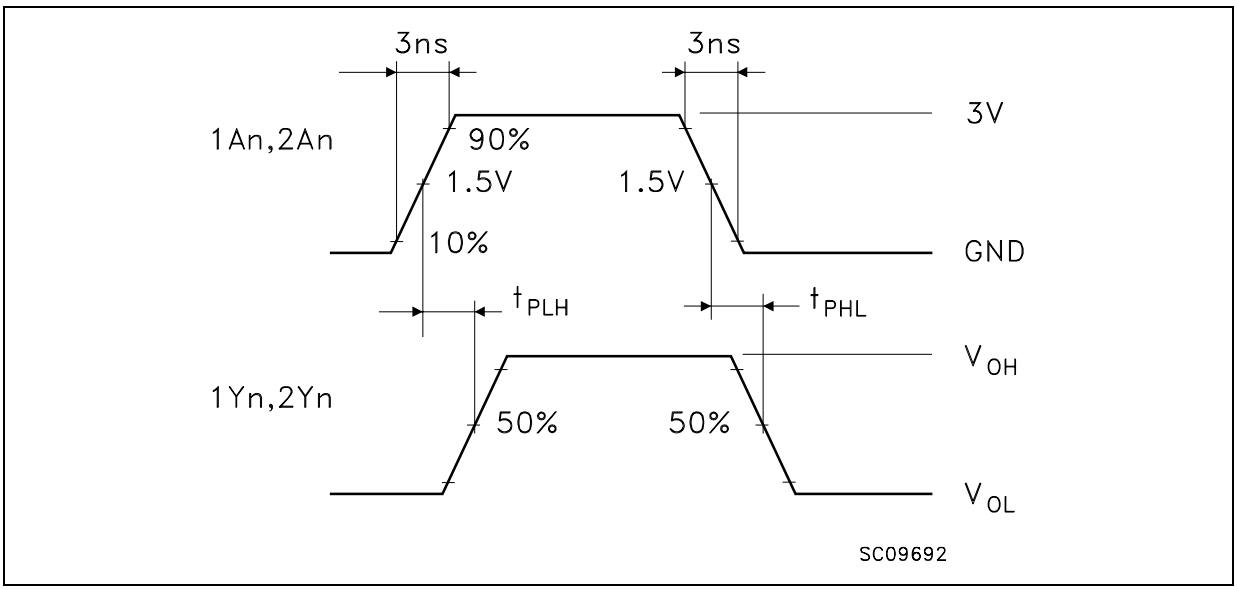
TEST CIRCUIT



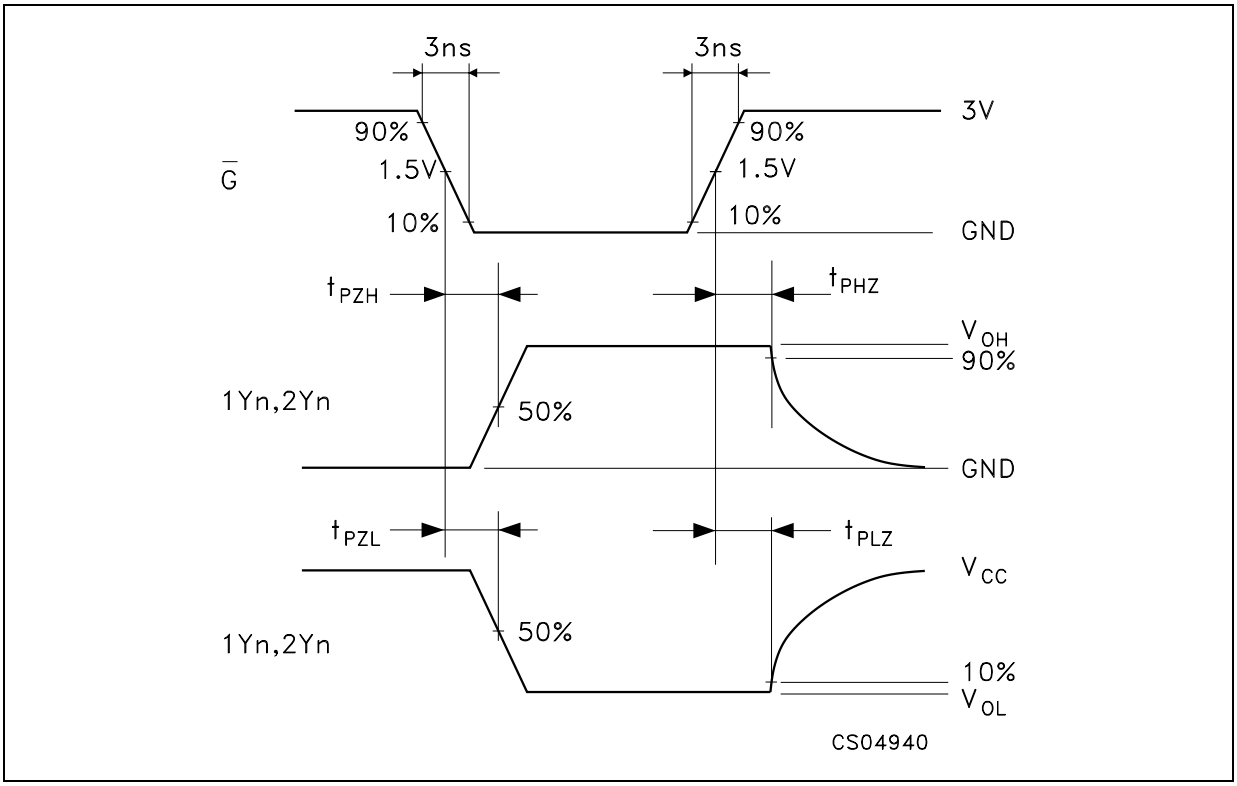
TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZLH}, t_{PLZ}	$2V_{CC}$
t_{PZH}, t_{PHZ}	Open

C_L = 50pF or equivalent (includes jig and probe capacitance)
$R_L = R_1$ = 500Ω or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

WAVEFORM 1: PROPAGATION DELAYS (f=1MHz; 50% duty cycle)

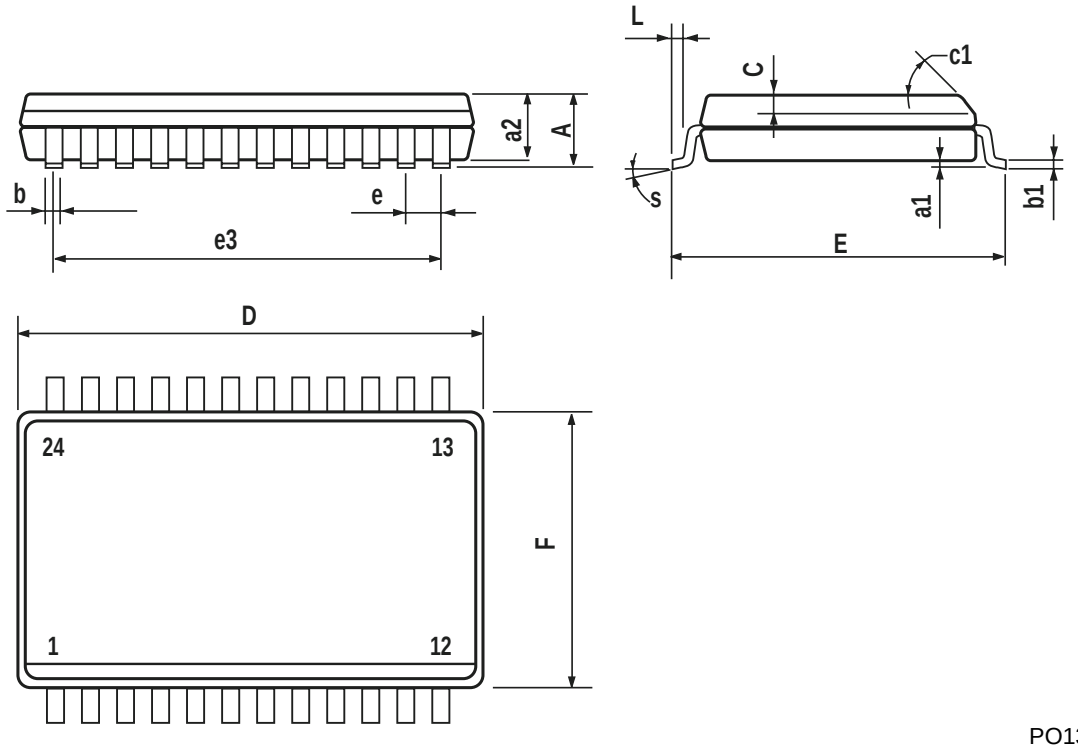


WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIME (f=1MHz; 50% duty cycle)



SO-24 MECHANICAL DATA

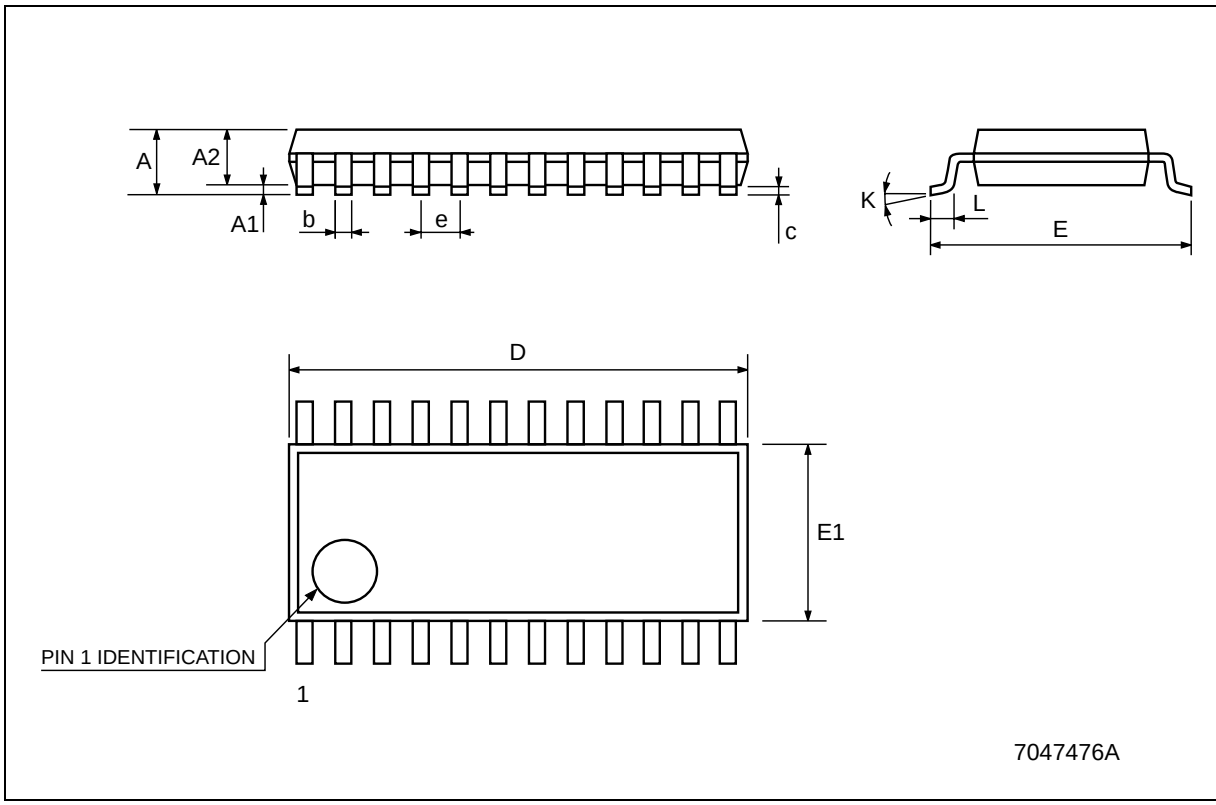
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45° (typ.)					
D	15.20		15.60	0.598		0.614
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		13.97			0.550	
F	7.40		7.60	0.291		0.300
L	0.50		1.27	0.020		0.050
S	8° (max.)					



PO13T

TSSOP24 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.1			0.043
A1	0.05		0.15	0.002		0.006
A2		0.9			0.035	
b	0.19		0.30	0.0075		0.0118
c	0.09		0.20	0.0035		0.0079
D	7.7		7.9	0.303		0.311
E	6.25		6.5	0.246		0.256
E1	4.3		4.5	0.169		0.177
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.50		0.70	0.020		0.028



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